AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A multiple-supply-voltage semiconductor device comprising:

a clock distribution circuit comprising:

at least one first block receiving a variable supply voltage, said at least one first block receiving a clock signal;

at least one second block receiving the variable supply voltage; and

at least one variable delay circuit which generates a delayed clock signal by ~~provides~~providing a delay in the clock signal received by the at least one first block, said delay changing in accordance with a change in the variable supply voltage provided to the at least one first block;

wherein the clock signal received by the at least one first block is different from ~~a~~ the delayed clock signal received by the at least one second block.

2. (currently amended): The multi-supply-voltage semiconductor device according to claim 1, wherein said at least one variable delay circuit includes circuitry to increase the delay as the variable supply voltage decreases.

3. (currently amended): A multi-supply-voltage semiconductor device comprising:

a clock distribution circuit comprising:

at least one first block receiving a variable supply voltage, said at least one first block receiving a clock signal;

at least one second block receiving the variable supply voltage;

a voltage level detector circuit which detects a voltage level of the variable supply voltage; and

at least one variable delay circuit which generates a delayed clock signal by ~~provides~~ providing a delay in the clock signal received by the at least one first block, said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit;

wherein the clock signal received by the at least one first block is different from ~~a~~ the delayed clock signal received by the at least one second block.

4. - 5. (canceled).

6. (currently amended): A multiple-supply-voltage semiconductor device comprising:

at least one block receiving a variable supply voltage, said at least one block receiving a clock signal;

at least one variable delay circuit which provides a delay in the clock signal received by the at least one block, said delay changing in accordance with a change in the variable supply voltage provided to the at least one block;

a voltage change detector circuit which detects a change in the variable supply voltage; and

a blocking unit that prevents the clock signal from being supplied to the at least one block during a period in which the voltage change detector circuit detects a change in the variable supply voltage.

7. (currently amended): A multiple-supply-voltage semiconductor device comprising:

at least one block receiving a variable supply voltage, said at least one block receiving a clock signal;

at least one variable delay circuit which provides a delay in the clock signal received by the at least one block, said delay changing in accordance with a change in the variable supply voltage provided to the at least one block;

a minimum voltage detector circuit which generates and outputs a power supply control signal which provides control to limit the variable supply voltage within a predetermined range; and

a power supply control circuit which controls the variable supply voltage in accordance with the power supply control signal.

8. - 9. (canceled).

10. (currently amended): The multi-supply-voltage semiconductor device according to claim 6, wherein said at least one variable delay circuit includes circuitry to increase the delay as the variable supply voltage decreases.

11. (currently amended): A multi-supply-voltage semiconductor device comprising:

at least one block receiving a variable supply voltage, said at least one block receiving a clock signal;

a voltage level detector circuit which detects a voltage level of the variable supply voltage;

at least one variable delay circuit which provides a delay in the clock signal received by the at least one block, said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit;

a voltage change detector circuit which detects a change in the variable supply voltage; and

a blocking unit that prevents the clock signal from being supplied to the at least one block during a period in which the voltage change detector circuit detects a change in the variable supply voltage.

12. - 13. (canceled).

14. (currently amended): The multi-supply-voltage semiconductor device according claim 7, wherein said at least one variable delay circuit includes circuitry to increase the delay as the variable supply voltage decreases.

15. - 17. (canceled).

18. (previously presented): A multiple-supply-voltage semiconductor device according to claim 1, wherein the at least one variable delay circuit comprises a multistage inverter comprising multiple inverters connected in series.

19. (previously presented): A multiple-supply-voltage semiconductor device according to claim 1, wherein the at least one variable delay circuit comprises a plurality of stacked inverter stages.

20. (previously presented): A multiple-supply-voltage semiconductor device according to claim 6, wherein said voltage change detector circuit comprises:

an analog to digital converter circuit;

a flip-flop circuit;

and a comparator.

21. (currently amended): A multiple-supply-voltage semiconductor device according to claim 20, wherein said comparator compares a first digital information held in said flip-flop circuit with a second digital information output from said analog to digital converter circuit, and detects a change in the variable supply voltage if said first and second digital information do not match.

22. (currently amended): A multi-supply-voltage semiconductor device comprising:

at least one block receiving a variable supply voltage, said at least one block receiving a clock signal;

a voltage level detector circuit which detects a voltage level of the variable supply voltage; and

at least one variable delay circuit which provides a delay in the clock signal received by the at least one block, said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit;

wherein said voltage level detector circuit comprises a differential amplifier into which the variable supply voltage and a reference voltage is input.

23. (currently amended): A multi-supply-voltage semiconductor device comprising:

at least one block receiving a variable supply voltage, said at least one block receiving a clock signal;

a voltage level detector circuit which detects a voltage level of the variable supply voltage; and

at least one variable delay circuit which provides a delay in the clock signal received by the at least one block, said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit;

wherein said at least one variable delay circuit comprises a selector and a delay gate, wherein the delay gate delays the clock signal and the selector outputs to the at least one block either the clock signal or the delayed clock signal generated by the delay gate.

24. (previously presented): A multiple-supply-voltage semiconductor device according to claim 23, wherein said delay gate comprises at least one inverter.

25. (currently amended): A multi-supply-voltage semiconductor device comprising:

a clock distribution circuit comprising:

at least one block receiving a variable supply voltage, said at least one block receiving a clock signal;

a voltage level detector circuit which detects a voltage level of the variable supply voltage; and

at least one variable delay circuit which provides a delay in the clock signal received by the at least one block, said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit;

wherein said at least one variable delay circuit comprises a selector and a plurality of delay gates, wherein each one of said plurality of delay gates provides a different delay to the clock signal and the selector outputs to the at least one block either the clock signal or one of the delayed clock signals generated by the delay gate.

26. (previously presented): A multiple-supply-voltage semiconductor device according to claim 23, wherein said delay gate comprises at least one inverter.

27. - 28. (canceled).

29. (previously presented): A multiple-supply-voltage semiconductor device according to claim 3, wherein the voltage level detector circuit outputs the detected voltage level as a voltage level detect signal.

30. (previously presented): A multiple-supply-voltage semiconductor device comprising:

at least one first block receiving a first variable supply voltage, said at least one first block receiving a clock signal;

at least one second block receiving a second supply voltage; and

at least one variable delay circuit which provides a delay in the clock signal received by the at least one second block, said delay changing in accordance with a change in the first variable supply voltage provided to the at least one first block;

wherein the clock signal received by the at least one first block is different from a clock signal received by the at least one second block, and

wherein the first variable supply voltage is different from the second supply voltage.

31. (currently amended): The multi-supply-voltage semiconductor device according to claim 30, wherein said at least one variable delay circuit includes circuitry to increase the delay as the variable supply voltage decreases.

32. (previously presented): A multi-supply-voltage semiconductor device comprising:

at least one first block receiving a first variable supply voltage, said at least one first block receiving a clock signal;

at least one second block receiving a second supply voltage;

a voltage level detector circuit which detects a voltage level of the first variable supply voltage; and

at least one variable delay circuit which provides a delay in the clock signal received by the at least one second block, said delay changing in accordance with a change in the voltage level detected by the voltage level detector circuit;

wherein the clock signal received by the at least one first block is different from a clock signal received by the at least one second block, and

wherein the first variable supply voltage is different from the second supply voltage.

33. (previously presented): A multiple-supply-voltage semiconductor device according to claim 30, wherein the at least one variable delay circuit comprises a multistage inverter comprising multiple inverters connected in series.

34. (previously presented): A multiple-supply-voltage semiconductor device according to claim 30, wherein the at least one variable delay circuit comprises a plurality of stacked inverter stages.

35. (previously presented): A multiple-supply-voltage semiconductor device according to claim 32, wherein the voltage level detector circuit outputs the detected voltage level as a voltage level detect signal.